Fig. 1 (Prior Art)

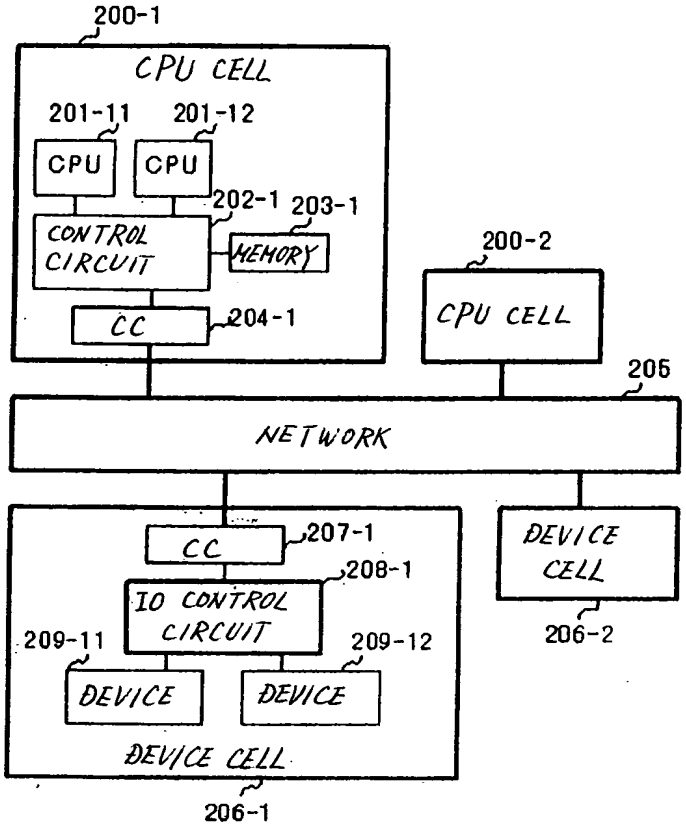


Fig. 2 (Prior Art)

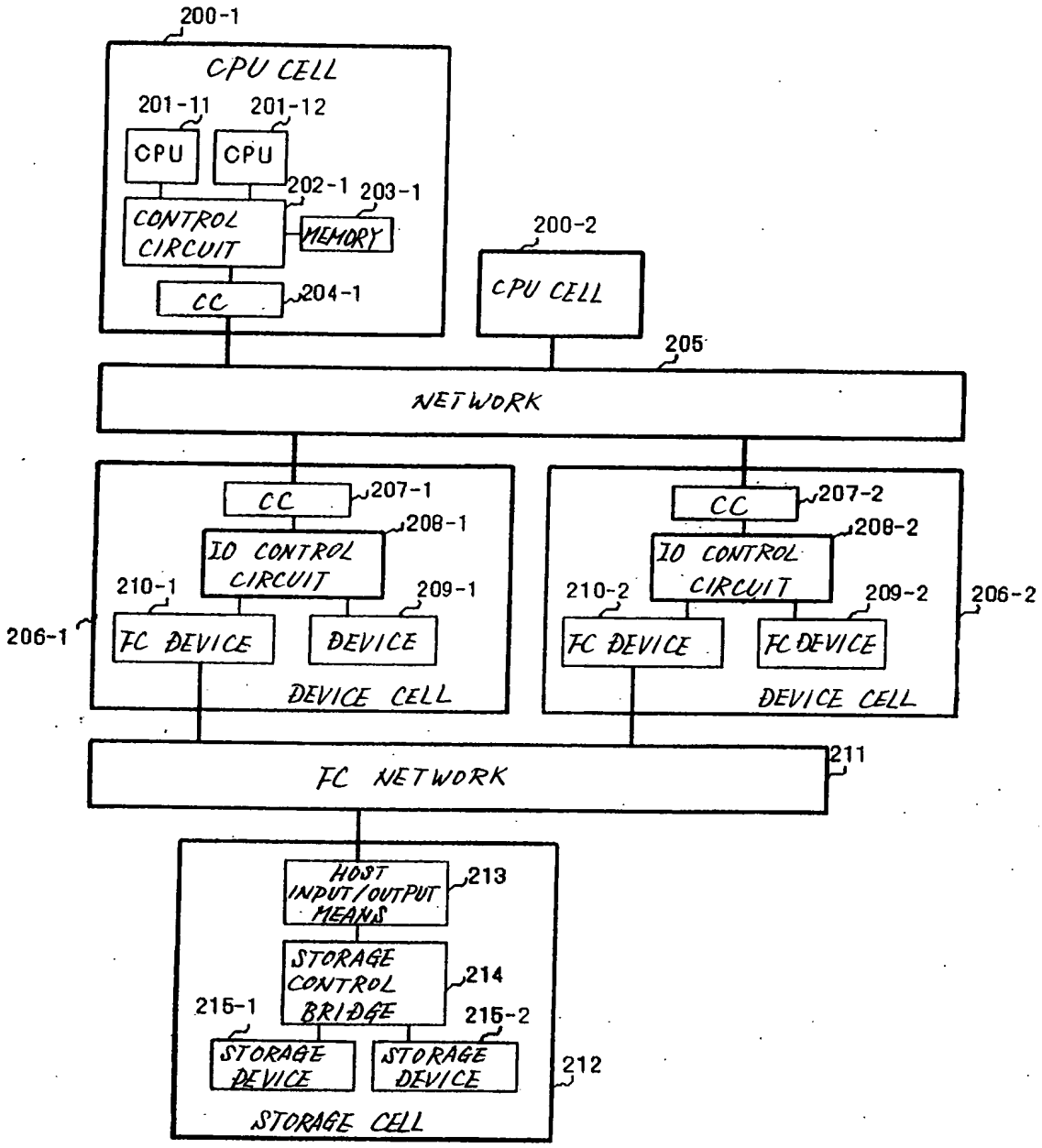


Fig. 3

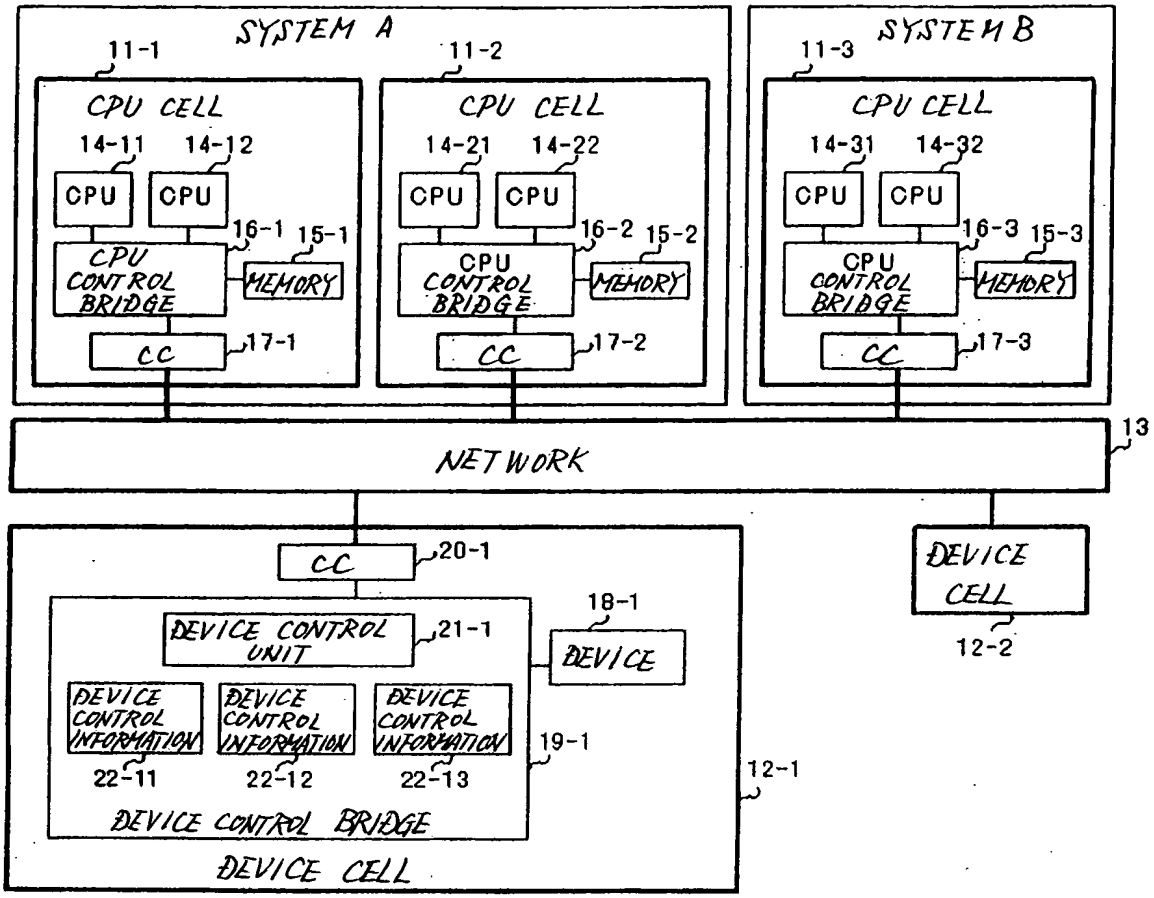



Fig. 4

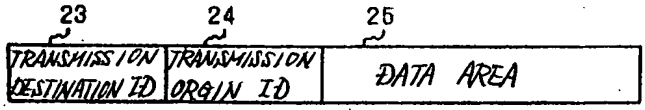



Fig. 5

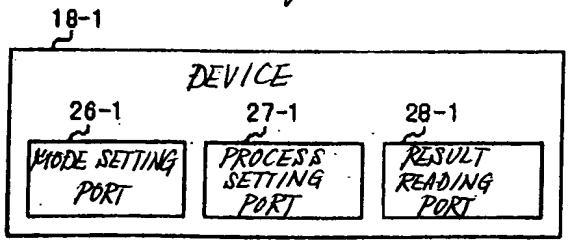


Fig. 6

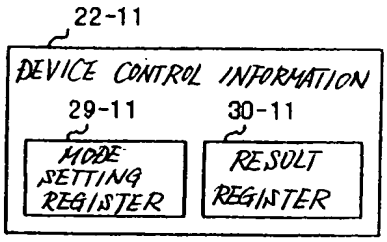

22-11
DEVICE CONTROL INFORMATION
29-11
30-11
MODE SETTING REGISTER
RESULT REGISTER

Fig. 7

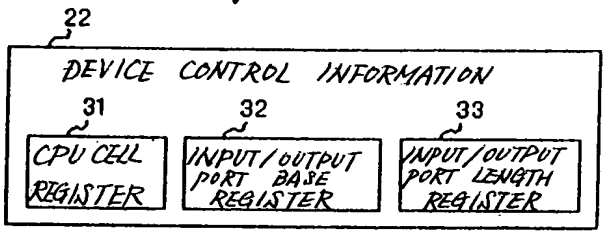

22
DEVICE CONTROL INFORMATION
31
32
33
CPU CELL REGISTER
INPUT/OUTPUT PORT BASE REGISTER
INPUT/OUTPUT PORT LENGTH REGISTER

Fig. 8

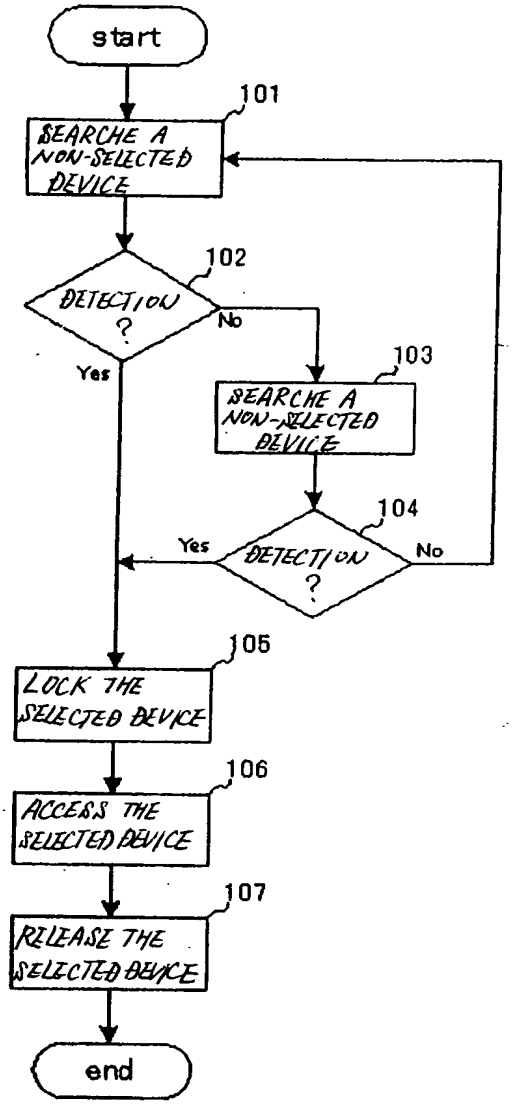

start
101
SEARCHE A NON-SELECTED DEVICE
102
DETECTION ?
No
Yes
103
SEARCHE A NON-SELECTED DEVICE
104
Yes
DETECTION ?
No
105
LOCK THE SELECTED DEVICE
106
ACCESS THE SELECTED DEVICE
107
RELEASE THE SELECTED DEVICE
end

Fig. 9

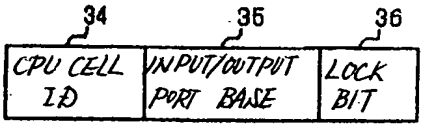

34
35
36
CPU CELL ID
INPUT/OUTPUT PORT BASE
LOCK BIT

Fig. 10

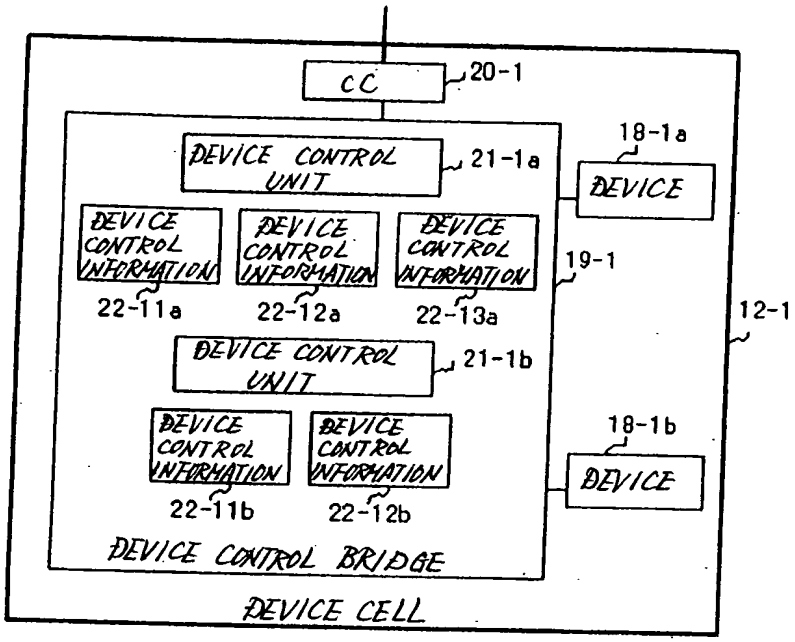



Fig. 11

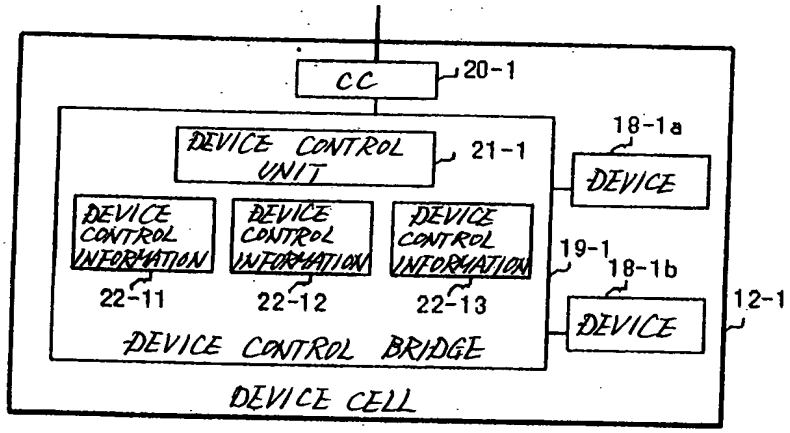



Fig. 12

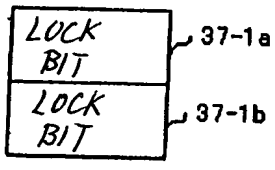


Fig. 13

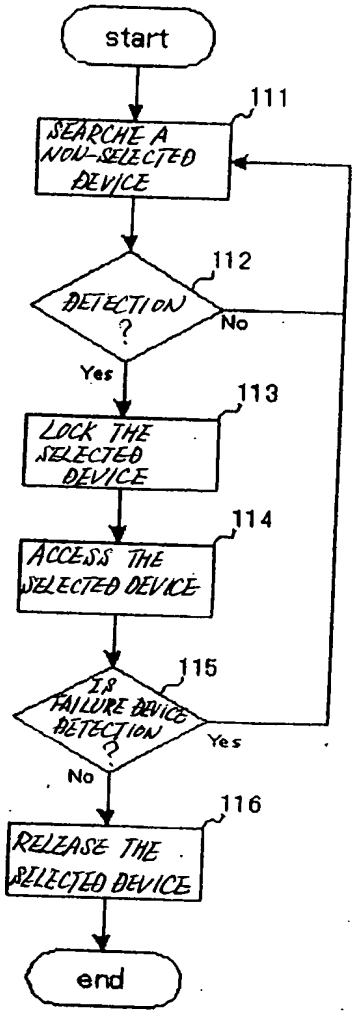

start
111
SEARCHE A NON-SELECTED DEVICE
112
DETECTION ?
No
Yes
113
LOCK THE SELECTED DEVICE
114
ACCESS THE SELECTED DEVICE
115
IS FAILURE DEVICE DETECTION ?
Yes
No
116
RELEASE THE SELECTED DEVICE
end

Fig. 14

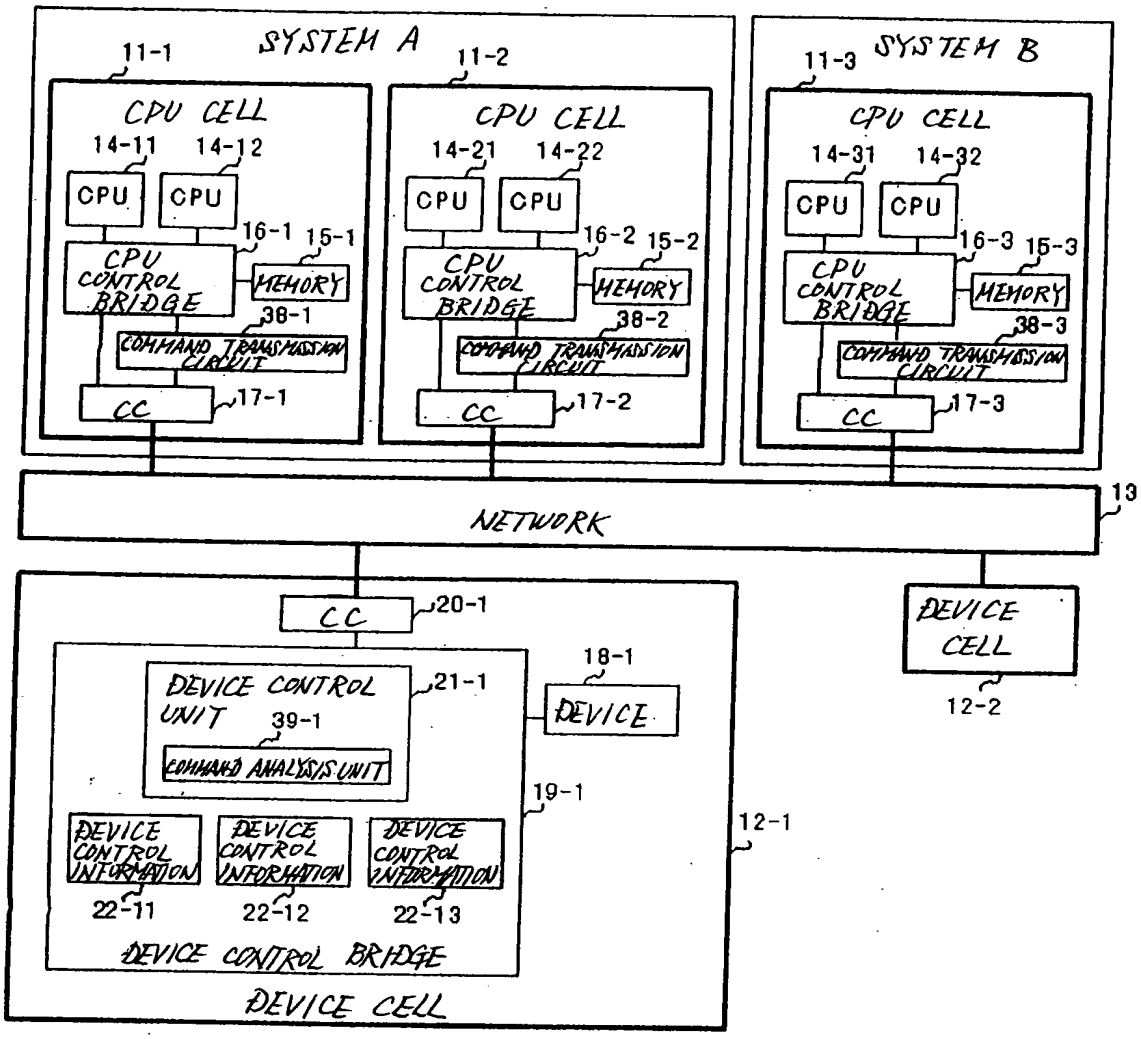
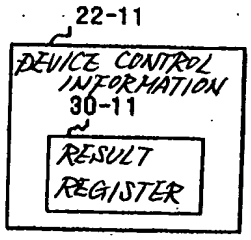

SYSTEM A
11-1
CPU CELL
14-11
14-12
CPU
CPU
16-1
15-1
CPU CONTROL BRIDGE
MEMORY
38-1
COMMAND TRANSMISSION CIRCUIT
CC
17-1
11-2
CPU CELL
14-21
14-22
CPU
CPU
16-2
15-2
CPU CONTROL BRIDGE
MEMORY
38-2
COMMAND TRANSMISSION CIRCUIT
CC
17-2
SYSTEM B
11-3
CPU CELL
14-31
14-32
CPU
CPU
16-3
15-3
CPU CONTROL BRIDGE
MEMORY
38-3
COMMAND TRANSMISSION CIRCUIT
CC
17-3
NETWORK
13
CC
20-1
DEVICE CONTROL UNIT
21-1
39-1
COMMAND ANALYSIS UNIT
18-1
DEVICE
19-1
DEVICE CONTROL INFORMATION
22-11
DEVICE CONTROL INFORMATION
22-12
DEVICE CONTROL INFORMATION
22-13
DEVICE CONTROL BRIDGE
DEVICE CELL
12-1
DEVICE CELL
12-2

Fig. 15


22-11
DEVICE CONTROL INFORMATION
30-11
RESULT REGISTER